

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT244**

**Octal buffer/line driver; 3-state**

Product specification  
File under Integrated Circuits, IC06

December 1990

## Octal buffer/line driver; 3-state

## 74HC/HCT244

## FEATURES

- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT244 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT244 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $1\overline{OE}$  and  $2\overline{OE}$ . A HIGH on  $n\overline{OE}$  causes the outputs to assume a high impedance OFF-state. The “244” is identical to the “240” but has non-inverting outputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	9	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	35	35	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

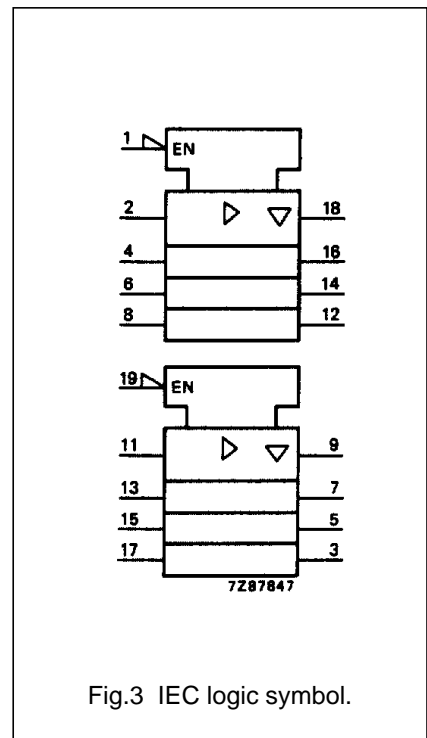
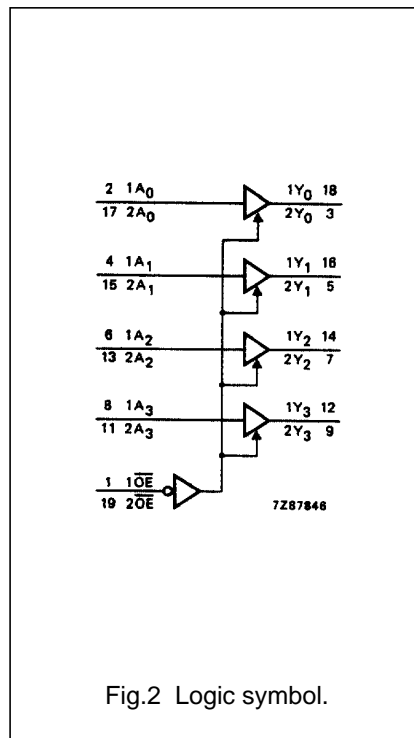
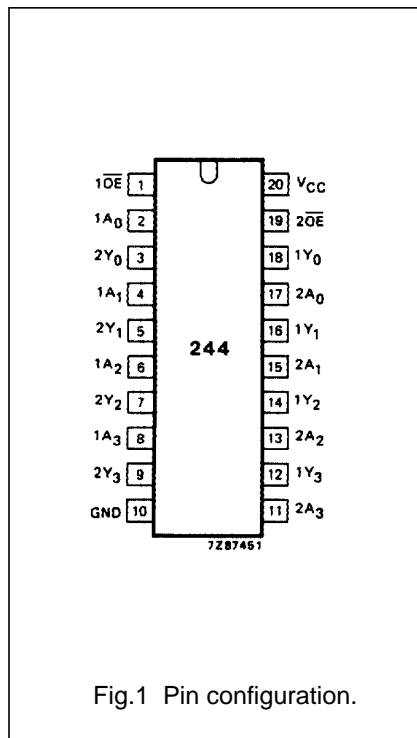
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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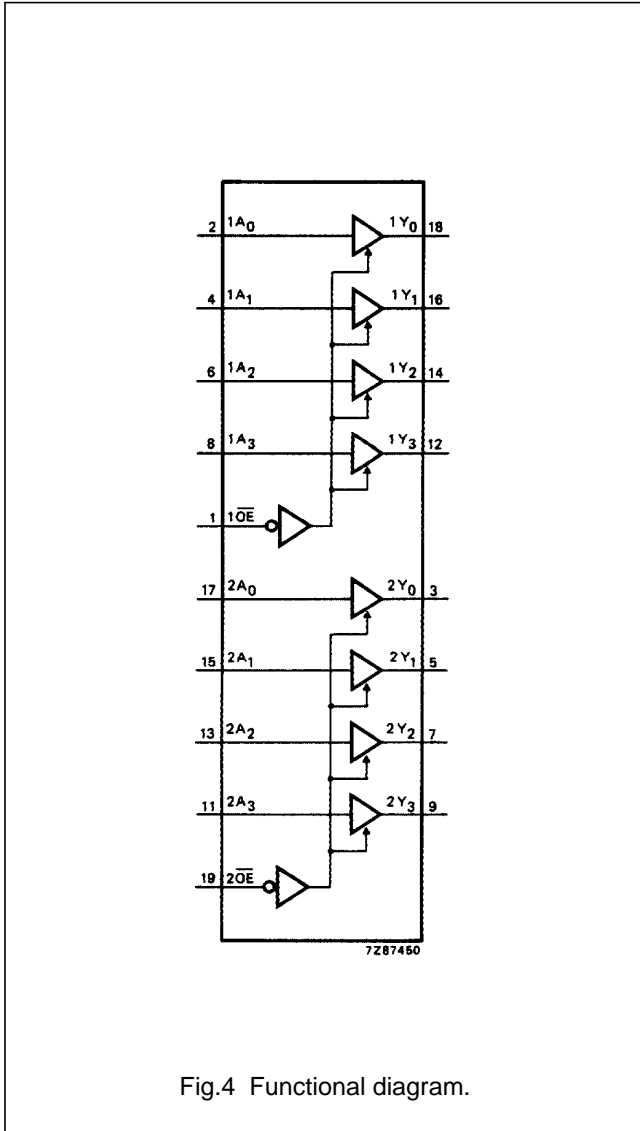
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{1OE}$	output enable input (active LOW)
2, 4, 6, 8	1A <sub>0</sub> to 1A <sub>3</sub>	data inputs
3, 5, 7, 9	2Y <sub>0</sub> to 2Y <sub>3</sub>	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A <sub>0</sub> to 2A <sub>3</sub>	data inputs
18, 16, 14, 12	1Y <sub>0</sub> to 1Y <sub>3</sub>	bus outputs
19	$\overline{2OE}$	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage



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FUNCTION TABLE

INPUTS		OUTPUT
$\overline{nOE}$	$nA_n$	$nY_n$
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		30 11 9	110 22 19		145 28 24		165 33 28	ns	2.0 4.5 6.0	Fig.5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1 $\overline{\text{OE}}$ to 1Y <sub>n</sub> ; 2 $\overline{\text{OE}}$ to 2Y <sub>n</sub>		36 13 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time 1 $\overline{\text{OE}}$ to 1Y <sub>n</sub> ; 2 $\overline{\text{OE}}$ to 2Y <sub>n</sub>		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5

## Octal buffer/line driver; 3-state

## 74HC/HCT244

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1A <sub>n</sub>	0.70
2A <sub>n</sub>	0.70
1 $\overline{OE}$	0.70
2 $\overline{OE}$	0.70

**AC CHARACTERISTICS FOR 74HCT**

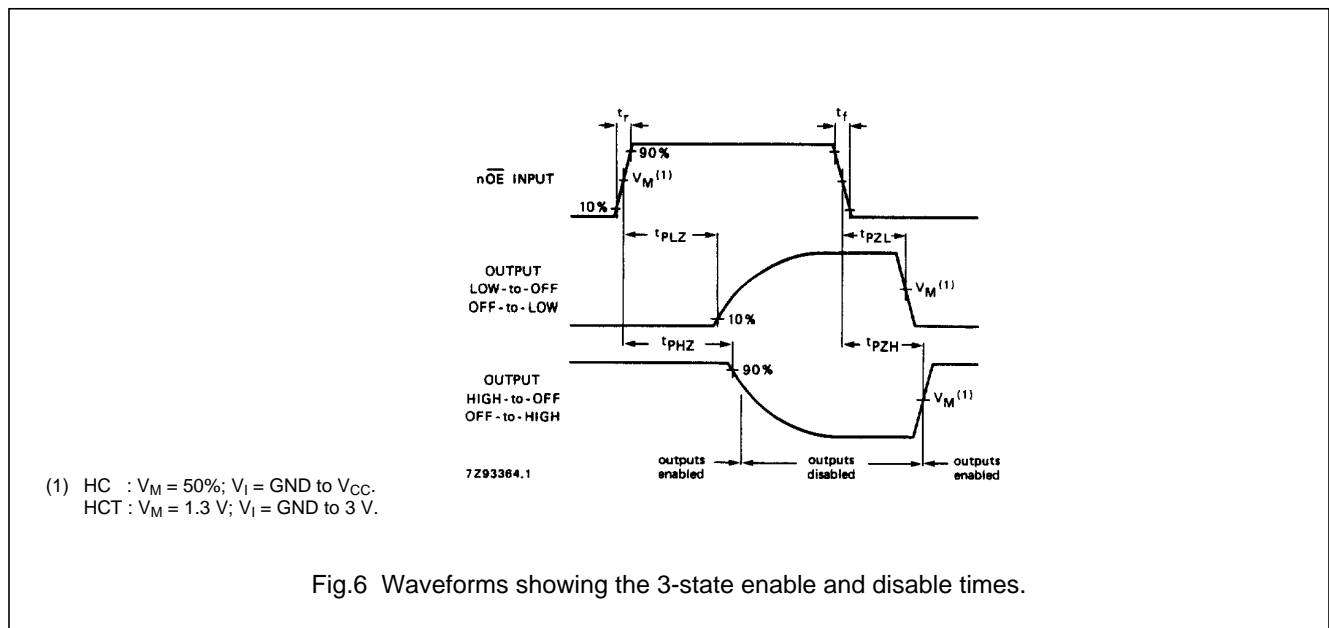
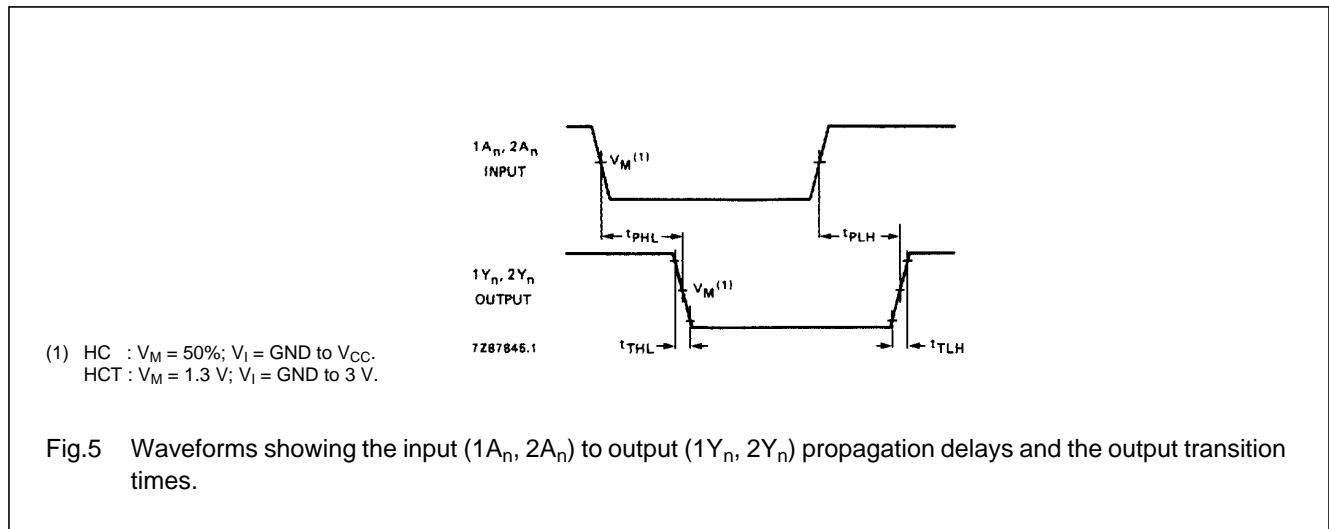
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		13	22		28		33	ns	4.5	Fig.5	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1 $\overline{OE}$ to 1Y <sub>n</sub> ; 2 $\overline{OE}$ to 2Y <sub>n</sub>		15	30		38		45	ns	4.5	Fig.6	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time 1 $\overline{OE}$ to 1Y <sub>n</sub> ; 2 $\overline{OE}$ to 2Y <sub>n</sub>		15	25		31		38	ns	4.5	Fig.6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.5	

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".