Data Sheet

Alphanumeric dot matrix liquid crystal displays

RS stock numbers 184-8392, 184-8415, 184-8421, 184-8803, 184-9042, 184-9058, 184-9070, 588-500, 588-516, 588-774, 588-796, 588-538, 588-803

Intelligent, alphanumeric, dot matrix modules with integral CMOS microprocessor and LCD display drivers. The modules utilise a 5 ×7 dot matrix format (except 16 × 1, which uses a 5 × 10 and 20 × 4 which uses 5 × 8), with cursor, and are capable of displaying the full ASCII character set plus up to 8 additional user programmable custom symbols. The displays are virtually burden free to the host processor. Internal registers store up to 80 characters and all update and refresh is internal. Software development is greatly eased by powerful, single step instructions which eliminate many lines of conventional coding.

Applications

- Telecommunications
- Medical instruments
- Hand-held terminals
- Electronic typewriters
- Point of sale terminals
- Test instruments
- Word processors.

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Features

- 5V, 2mA, single power supply
- High contrast, dot matrix characters for good readability
- Wide adjustable viewing angle
- Compact and lightweight
- TTL and 5V CMOS compatible
- Interfaces to 4 or 8-bit data busses
- Powerful instructions
- Display ‘Blank’, ‘Flash’ or ‘Flash Limited Area’
- ASCll compatible
- 160 different alphanumeric characters and symbols
- 8-user programmable RAM locations for custom symbols
- 80-character memory allows easy scrolling or general purpose storage
- Cursor ‘Flash’, or off
- Automatic display shift – simple command structure
- Scrolls left or right or alternates complete lines.

Figure 1 Module block diagrams

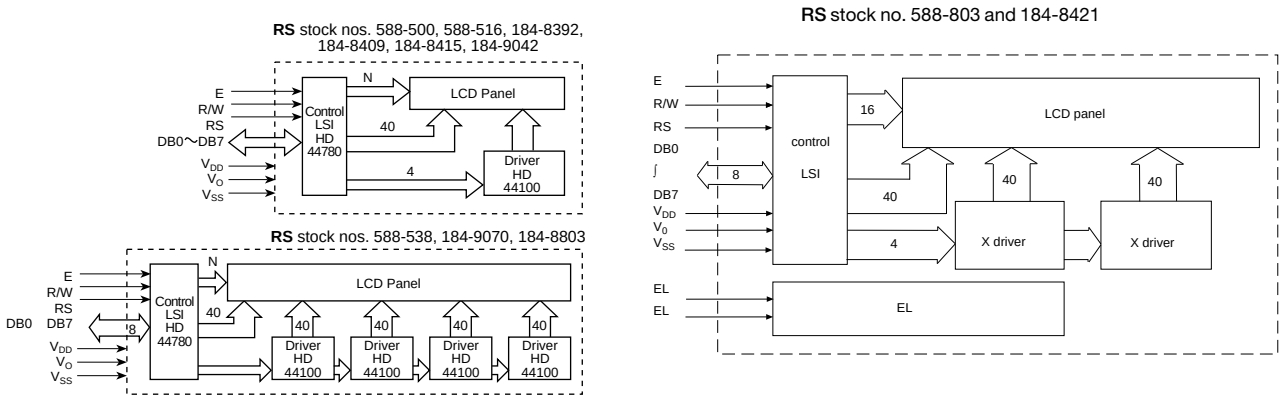
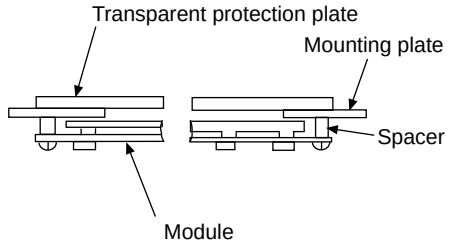


Figure 2 Typical module mounting



Absolute maximum ratings

Item	Symbol	Min.	Max.
Logic circuit power supply voltage*	V_{DD}-V_{SS}	0V	7.0V
LC driver circuit supply voltage†	V_{DD}-V_O	0V	13.5V
Input voltage	V_I	V_{SS}	V_{DD}
Operating temp.		0°C	+50°C
Storage temp. (all TN types)		–20°C	+70°C
Storage temp. (all STN types)		–20°C	+60°C

* Reverse polarity connection to the logic circuit will cause irreparable damage.
† Instantaneous value.

Electro-optical characteristics $V_{DD} = 5.0 \pm 0.25V$, $T_a = 25°C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input 'High' voltage	V_{IH}		2.2	–	V_{DD}	V
Input 'Low' voltage	V_{IL}		–0.3	–	0.6	V
Output 'High' voltage	V_{OH}	$-I_{OH} = 0.205mA$	2.4	–	–	V
Output 'Low' voltage	V_{OL}	$I_{OL} = 1.6mA$	–	–	0.4	V
1 line module drive voltage (1/8 duty) 5 ×7 font + cursor	V_{DD}-V_O	$T_a = 0°C$ $T_a = 25°C$ $T_a = 50°C$	4.2 3.8 3.4	4.3 3.9 3.5	4.4 4.0 3.6	V V V
2 line module drive voltage (1/16 duty) 5 ×7 font + cursor	V_{DD}-V_O	$T_a = 0°C$ $T_a = 25°C$ $T_a = 50°C$	4.8 4.3 3.8	4.9 4.4 3.9	5.0 4.5 4.0	V V V
Viewing angle	ø1-ø2	K = 1.4	20	–	–	deg.
Contrast ratio	K	ø = 20°, 0 = 0°	3	–	–	
Rise time	tr	ø = 20°	–	150	250	ms
Fall time	tf	ø = 20°	–	150	250	ms

Power supply current I_{DD}

Display type	Size	Typ.	Max.	Units
TN and STN	2 × 8	0.8	2.0	mA
	1 × 16, 2 × 16, 2 × 24, 2 × 40	1.0	3.0	mA
	2 × 20, 4 × 20	2.0	5.0	mA
	4 × 40	4.0	10.0	mA

Figure 3 **Definition**

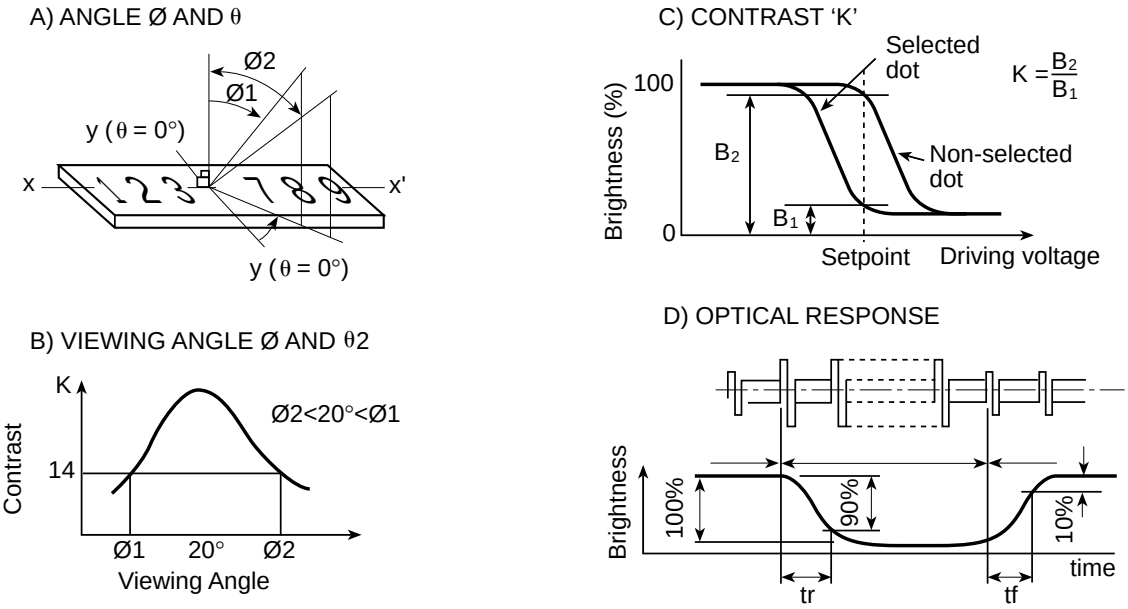
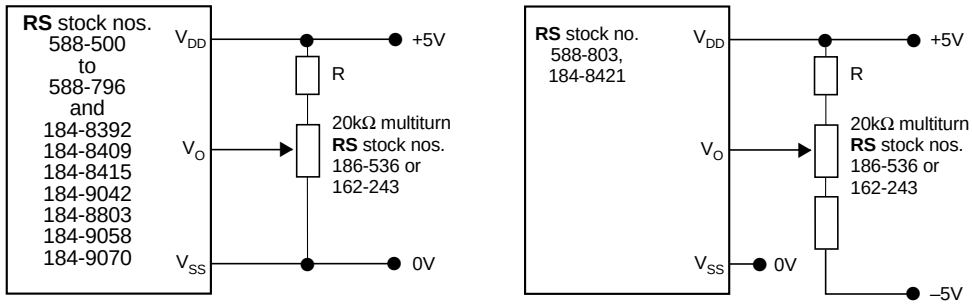


Figure 4 **Power supply**



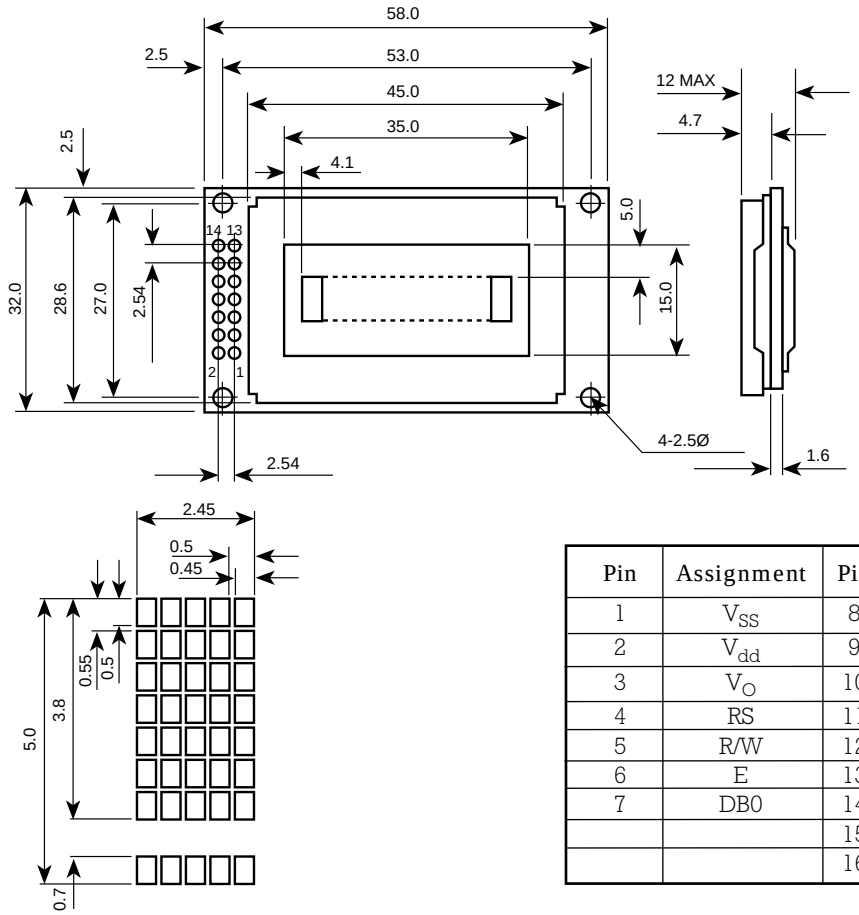
Viewing angle control V_O x 0.7V

Viewing angle control V_O x –2.7V to –2.9V

Padding resistor(s) may be required to limit voltage swing at V_O.

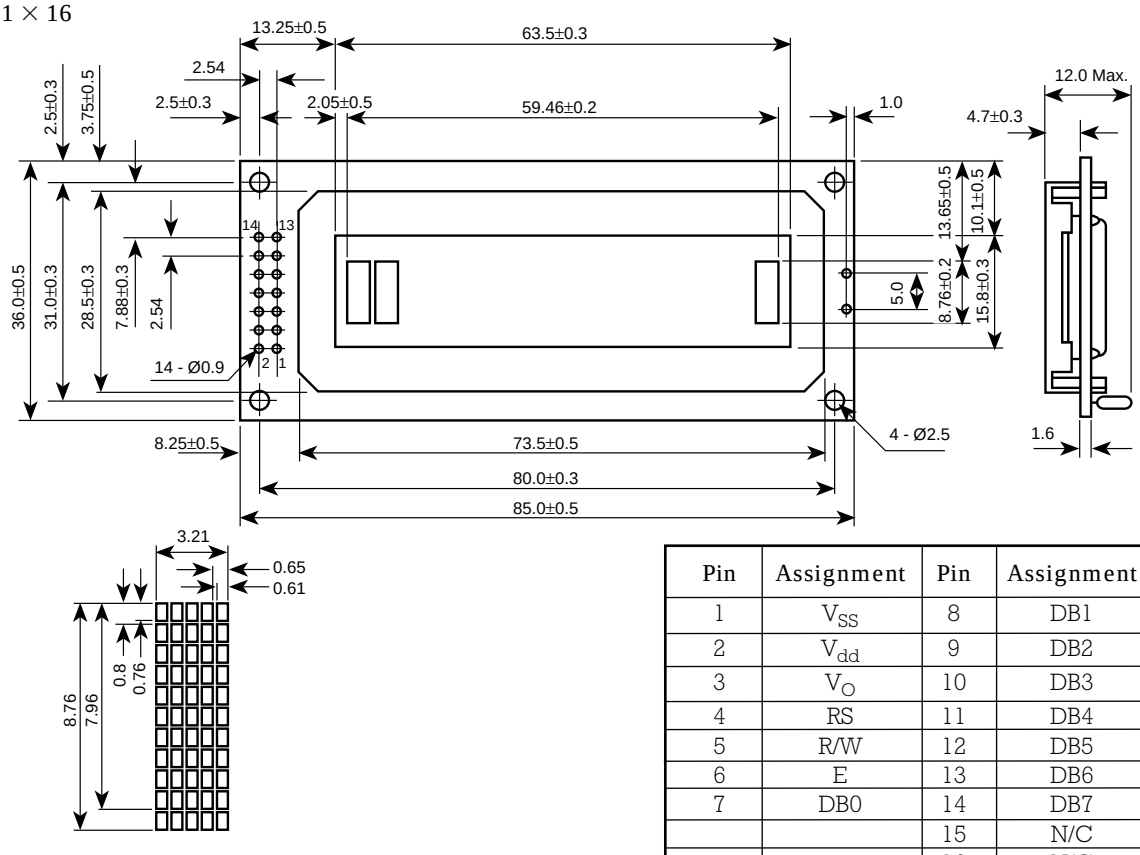
Mechanical dimensions

Figure 5 2 × 8



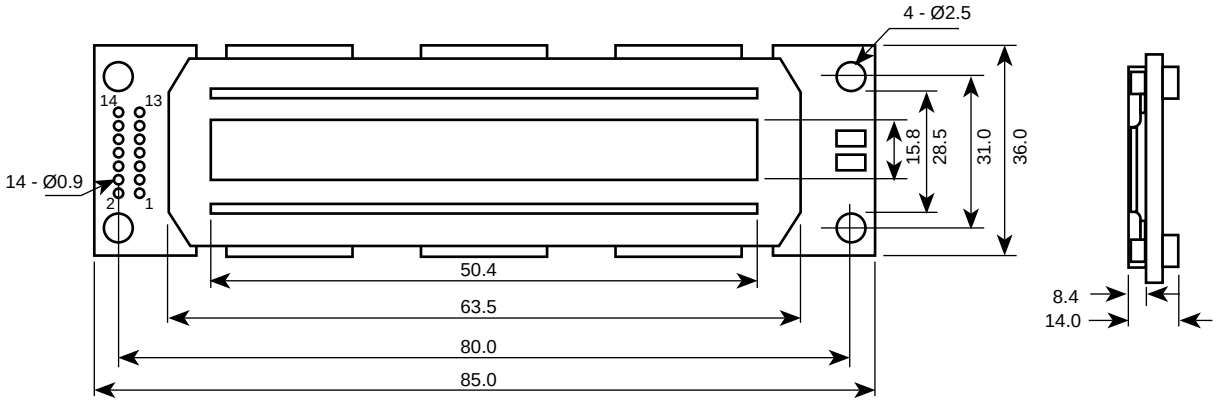
Pin	Assignment	Pin	Assignment
1	V_{SS}	8	DB1
2	V_{dd}	9	DB2
3	V_O	10	DB3
4	RS	11	DB4
5	R/W	12	DB5
6	E	13	DB6
7	DB0	14	DB7
		15	N/C
		16	N/C

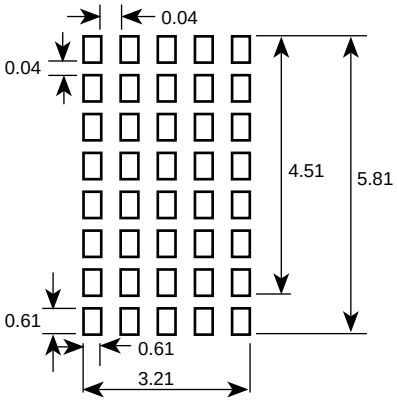
Figure 6 1 × 16



Pin	Assignment	Pin	Assignment
1	V_{SS}	8	DB1
2	V_{dd}	9	DB2
3	V_O	10	DB3
4	RS	11	DB4
5	R/W	12	DB5
6	E	13	DB6
7	DB0	14	DB7
		15	N/C
		16	N/C

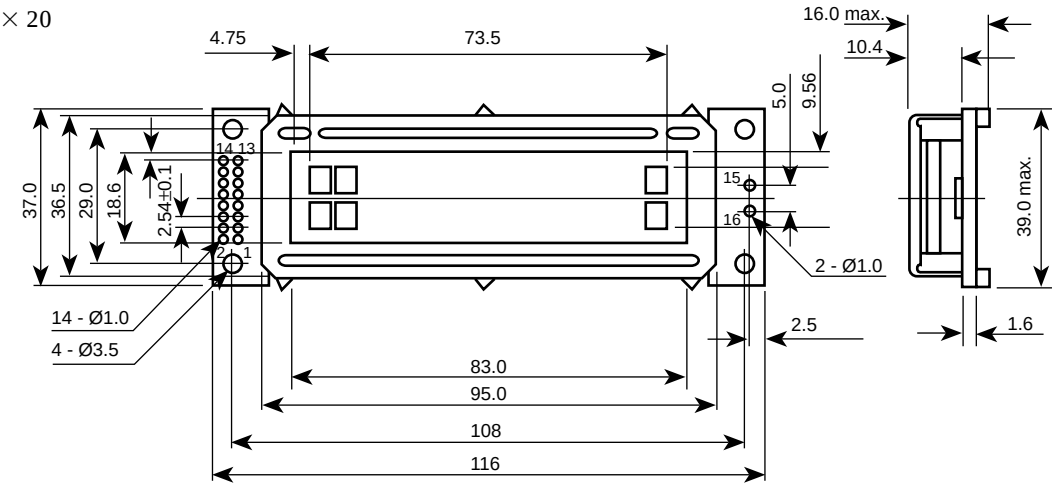
Figure 7 2 × 16

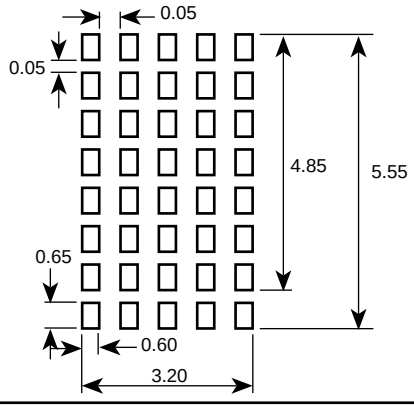




Pin	Assignment	Pin	Assignment
1	V_{SS}	8	DB1
2	V_{dd}	9	DB2
3	V_O	10	DB3
4	RS	11	DB4
5	R/W	12	DB5
6	E	13	DB6
7	DB0	14	DB7
		15	N/C
		16	N/C

Figure 8 2 × 20

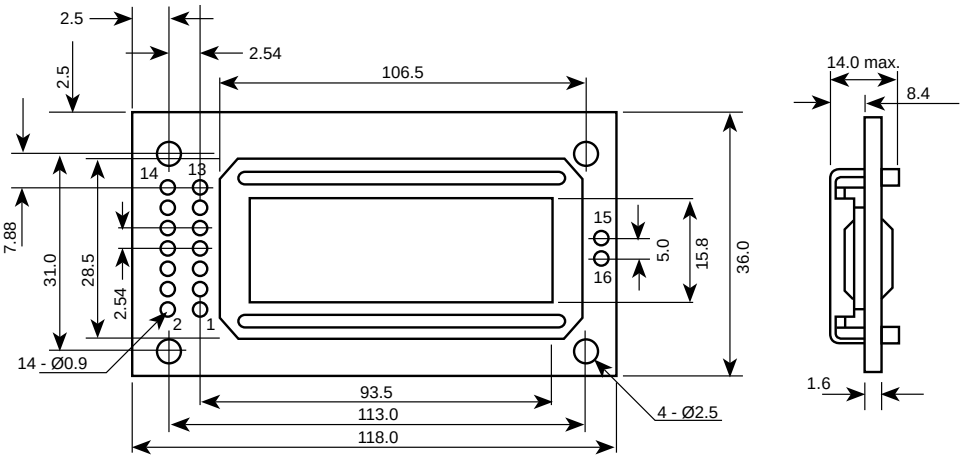


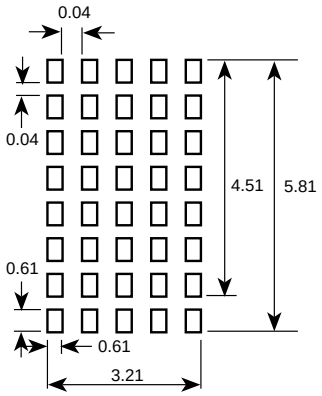


Pin	Assignment	Pin	Assignment
1	V_{SS}	9	DB2
2	V_{dd}	10	DB3
3	V_O	11	DB4
4	RS	12	DB5
5	R/W	13	DB6
6	E	14	DB7
7	DB0	15	N/C
8	DB1	16	N/C

Mechanical dimensions

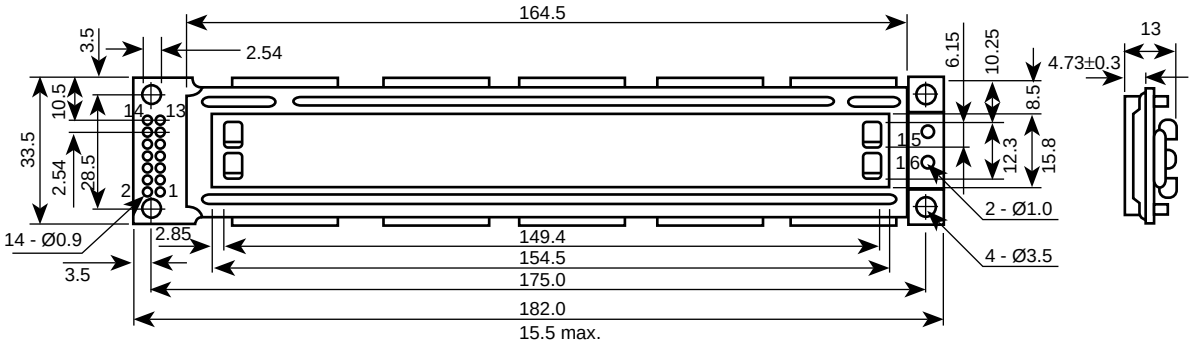
Figure 9 2 × 24

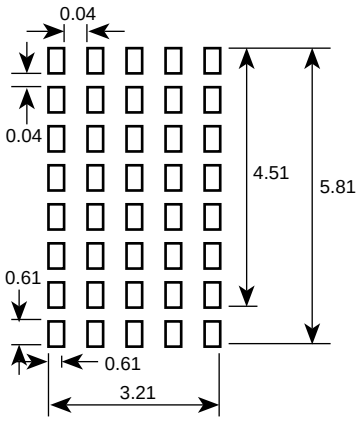




Pin	Assignment	Pin	Assignment
1	V_{SS}	9	DB2
2	V_{dd}	10	DB3
3	V_O	11	DB4
4	RS	12	DB5
5	R/W	13	DB6
6	E	14	DB7
7	DB0	15	N/C
8	DB1	16	N/C

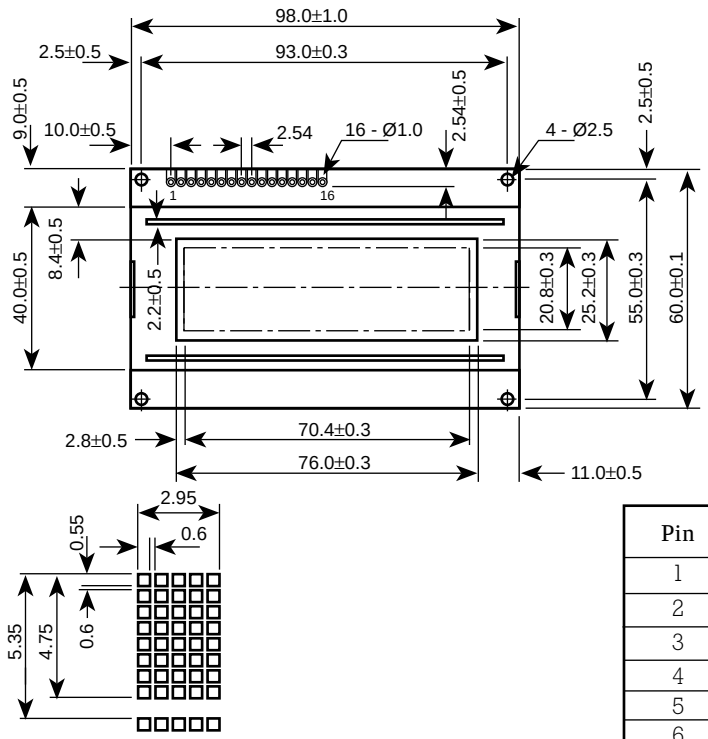
Figure 10 2 × 40





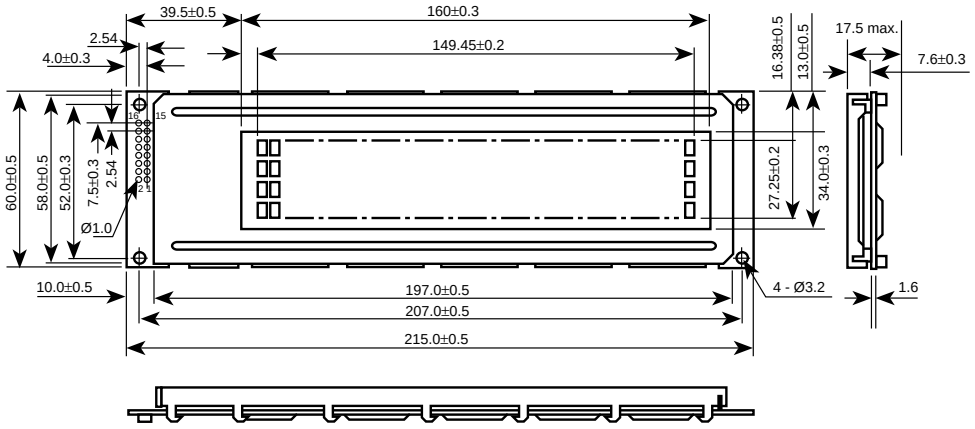
Pin	Assignment	Pin	Assignment
1	V_{SS}	9	DB2
2	V_{dd}	10	DB3
3	V_O	11	DB4
4	RS	12	DB5
5	R/W	13	DB6
6	E	14	DB7
7	DB0	15	N/C
8	DB1	16	N/C

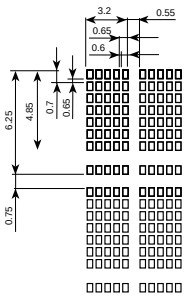
Figure 11 4 × 20



Pin	Assignment	Pin	Assignment
1	V_{SS}	9	DB2
2	V_{dd}	10	DB3
3	V_O	11	DB4
4	RS	12	DB5
5	R/W	13	DB6
6	E	14	DB7
7	DB0	15	N/C
8	DB1	16	N/C

Figure 12 4 × 40





Pin	Assignment	Pin	Assignment
1	DB6	9	E1
2	DB7	10	E2
3	DB4	11	RS
4	DB5	12	R/W
5	DB2	13	V_O
6	DB3	14	V_{DD}
7	DBO	15	N/C
8	DB1	16	N/C

RS stock no. 585-056
RS stock no. 184-8500

Font table

UPPER 4 BIT HEXADECIMAL

LOWER 4 BIT HEXADECIMAL

	Higher -Order Bits 4 bit / Lower-Order Bits 4 bit	0	2	3	4	5	6	7	A	B	C	D	E	F
		0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0	xxxx0000	CG RAM (1)												
1	xxxx0001	(2)												
2	xxxx0010	(3)												
3	xxxx0011	(4)												
4	xxxx0100	(5)												
5	xxxx0101	(6)												
6	xxxx0110	(7)												
7	xxxx0111	(8)												
8	xxxx1000	(1)												
9	xxxx1001	(2)												
A	xxxx1010	(3)												
B	xxxx1011	(4)												
C	xxxx1100	(5)												
D	xxxx1101	(6)												
E	xxxx1110	(7)												
F	xxxx1111	(8)												

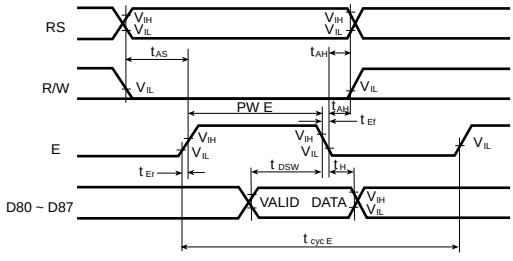
Instructions

Instruction	Code										Description	Execution time (f_{cp}(f_{osc}) = 250kHz
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears the display and returns the cursor to the home position (Address 0)	82µs ~1.64ms
Return home (cursor)	0	0	0	0	0	0	0	0	1	X	Returns the cursor to the home position (Address 0). A shifted display will also be restored to its original position. DD RAM contents remain unchanged	40µs ~1.6ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor direction and display shift. Operations are performed during data write and read	40µs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Selects display ON/OFF (D), cursor ON/OFF (C), and flash of cursor position character (B)	40µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	X	X	Moves the cursor shifts and/or the display without changing DD RM contents	40µs
Function set	0	0	0	0	1	DL	N	F	X	X	Sets interface data mode (DL), number of display lines (L), and character font (F)	40µs
Set CG RAM address	0	0	0	1	A_{CG}						Selects CG RAM address. Following this instruction all data is stored in/read from CG RAM	40µs
Set DD RAM address	0	0	1	A_{DD}							Selects DD RAM address. Following this instruction all data is stored in/read from DD RAM	40µs
Read Busy Flag and Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents	1.0µs
Write data to CG or DD RAM	1	0	Write data								Writes data into DD RAM or CG RAM	40µs
Read data to CG or DD RAM	1	1	Read data								Reads data from DD RAM or CG RAM	40µs
	I/D = 1: Increment I/D = 0: Decrement S = 1: Enable S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bit mode DL = 0: 4 bit mode N = 1: 2 lines N = 0: 1 line F = 1: Not used F = 0: 5×7 dots BF = 1: Display processor ready BF = 0: Ready for next instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address (Corresponds to cursor address) AC: Address counter, both DD and CG RAM addresses	

X = Don't care

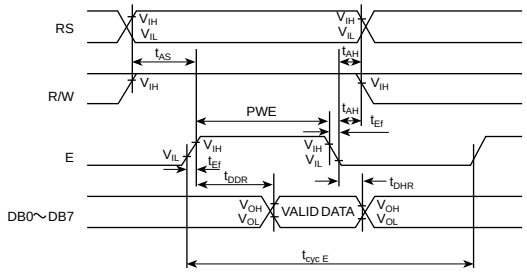
Timing characteristics

Figure 13 **Write operation**



Item	Symbol	Min.	Typ.	Max.	Unit
Enable Cycle Time	$t_{cyc\ E}$	1.0	-	-	µs
Enable Pulse Width	PW E	450	-	-	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	-	-	25	ns
Address Set-up Time	t_{AS}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Set-up Time	t_{DSW}	195	-	-	ns
Data Hold Time	t_H	10	-	-	ns

Figure 14 Read operation

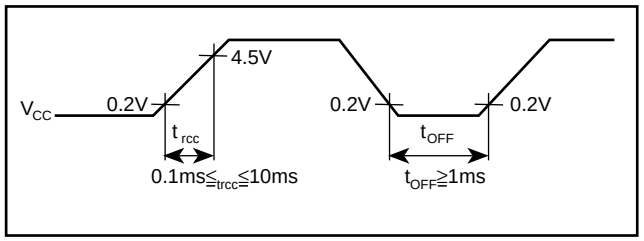


Reset function

The module has internal circuitry to initialise itself automatically upon the application of power. The reset sequence followed is:

1. Clear display
   The busy flag is set (BF = 1) during initialisation (approx. 15ms).
2. Function set .....DL = 1 : 8 bit wide interface mode
   N = 0 : 1-line display
   F = 0 : 5×7 dot character font
3. Display ON/OFF control.....D = 0 : Display OFF
   C = 0 : Cursor OFF
   B = 0 : Flash OFF
4. Entry mode set.....I/O = 1 : +1 (increment)
   S = 0 : No shift
5. DD RAM is selected

The display module power supply must have the following timing characteristic for the internal initialisation circuitry to function correctly.



Note: tOFF must be observed, particularly in the case of momentary power interruption, to ensure orderly initialisation of the module. If this restriction is not adhered to, the interface mode will be undefined and must first be set up to allow further initialisation commands to be recognised. The function set instruction, sent three times, will always select the 8-bit wide interface mode.

Function set:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	X	X	X
0	0	0	0	1	1	X	X	X	X

X = Don't care

When this instruction is sent, the module enters the 8-bit data length mode without fail.

Instruction description

Outline

Only two registers of the module, the Instruction Register (IR) and the Data Register (DR) can be controlled by the MPU directly. Control information is temporarily stored in these registers, prior to execution to allow interface to various types of MPUs which operate at different speeds from the module or to allow interface to peripheral control ICs. Internal operation is determined by signals sent from the host MPU, including register selection signals (RS), read/write signals (R/W) and data bus signals (DB0 = DB7). The table on page 6 shows the instructions and their execution times.

Details are explained in the following sections. The instructions can be divided into the following 4 types:

1. Instructions that designate the functions such as display format, data mode, etc.
2. Instructions that give internal RAM addresses.
3. Instructions that perform data transfer with internal RAM.
4. Other utility instructions.

In normal use, instructions of category (3), (to send display data), are used most frequently. Internal RAM addresses are configured to be automatically incremented (or decremented) by +1 after each data write, and hence the program overhead on the host MPU is reduced. Display Shift can be selected to occur with Display Write to further reduce this load. High speed ([a]50kHz) operation can be maintained by monitoring the busy flag (DB7).

Clear display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Writes ASCII space code '20' (hexadecimal) into all the DD RAM addresses. The cursor returns to Address 0 (Add = '80') and the display, if it has been shifted, returns to the original position. In other words, the display disappears and the cursor goes to the left edge of the display (the first line if 2 lines are displayed).

Return home (Cursor)

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	X

X = (Don't care)

Returns the cursor to Address 0 (ADD = '8Δ') and the display, if it has been shifted, to the original position. The DD RAM contents remain unchanged.

Entry mode set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by one upon writing into or reading a character code from the DD RAM. The cursor moves to the right when incremented by one. The same applies when writing and reading CG RAM data.

S: Shifts the entire display to either the right or the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Therefore, the cursor appears static with the display moving. The display is not shifted when reading from the DD RAM or when S = 0.

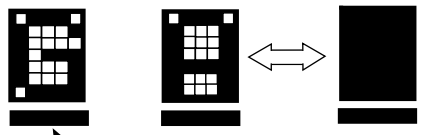
Display On/Off control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

D: Display is turned ON when D = 1 and OFF when D = 0. When display is turned off the display data remains in the DD RAM and it can be recalled at any time by setting D = 1.

C: The cursor is displayed when C = 1 and not displayed when C = 0. With the cursor disabled all internal operations (eg. I/D) function normally during a display data write. The cursor is displayed using 5 dots in the 8th character row.

B: The cursor character flashes at approx. 2.5Hz when B = 1. The cursor and flash enable can be set simultaneously.



(a) Cursor display example

(b) Flashing display example (Cursor enabled)

Cursor or shift display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	S/C	R/L	X	X

X = (Don't care)

Shifts the cursor position or display to the right or the left without writing or reading the display data. This function is used for correction or search of the display.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. (The cursor follows the display shift.)
1	1	Shifts the entire display to the right. (The cursor follows the display shift.)

Function set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	I/D	X

X = (Don't care)

DL: Sets interface data mode. Data is sent or received in 8 bit (using DB_7~DB_0) when DL = 1 or 4 bit words (using DB_7~DB_4) when DL = 0. When the 4 bit mode is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

N	F	No. of display lines	Character font	Duty cycle
0	0	1	5 ×7 dots	1/8
1	X	2	5 ×7 dots	1/16

X = (Don't care)

Set CG RAM address

	RS	R/W	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A
				←Higher order bits						Lower order bits →

Places the binary number AAAAAA into the address counter (AC) and refers all following data transfers to CG RAM.

Set DD RAM address

	RS	R/W	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A
				←Higher order bits						Lower order bits →

Places the binary number AAA ←AAAA into the address counter (AC) and refers all following data transfers to DD RAM. For a one line display (N = 0) valid addresses range from '00' →4F" (hexadecimal). For a two line display (N = 2) the first line is addressed from '00' →27' and the second from '40' →67' (hexadecimal).

Read Busy Flag and address

	RS	R/W	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A

←Higher order bits Lower order bits →

Reads Busy Flag (BF) and current Address Counter (AC) contents. When BF = 1, an internal operation is in progress and the next instruction is not accepted until BF is cleared to '0'. Check the BF status before attempting a write operation. At the same time, the value of the address counter is read as a binary number AAAAAA. The address counter is used by both CG and DD RAM and its value is determined by previous instructions. Address contents are those of the CG RAM or DD RAM last used.

Write Data to CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

←Higher order bits Lower order bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. The destination of the data is defined by the last 'set RAM address' instruction. After a Write Data instruction, an address adjust or display shift occurs as defined by Entry Mode.

Read Data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

←Higher order bits Lower order bits →

Reads binary 8 bit data DDDDDDDD from the CG or the DD RAM. The source of the data is defined by the last 'set RAM address' instruction. If a Read Data is attempted before execution of a set RAM address instruction then the data returned to the MPU is invalid. After a Read Data instruction, an address adjust occurs as defined by Entry Mode but the display shift is not actioned.

Table 2 **Relation between CG RAM addresses, Character Codes (DD RAM) and Character Patterns (CG RAM data)**

Character codes (DD RAM data) 7 6 5 4 3 2 1 0 (Higher-order bits → / Lower-order bits)	CG RAM address 5 4 3 2 1 0 (Higher-order bits → / Lower-order bits)	Character patterns (CG RAM data) 7 6 5 4 3 2 1 0 (Higher-order bits → / Lower-order bits)	
0 0 0 0 X 0 0 0	0 0 0	0 0 0	X X X 1 1 1 1 0
		0 0 1	X X X 1 0 0 0 1
		0 1 0	X X X 1 0 0 0 1
		0 1 1	X X X 1 1 1 1 0
		1 0 0	X X X 1 0 1 0 0
		1 0 1	X X X 1 0 0 1 0
		1 1 0	X X X 1 0 0 0 1
		1 1 1	X X X 0 0 0 0 0
0 0 0 0 X 0 0 1	0 0 1	0 0 0	X X X 1 0 0 0 1
		0 0 1	X X X 0 1 0 1 0
		0 1 0	X X X 1 1 1 1 1
		0 1 1	X X X 0 0 1 0 0
		1 0 0	X X X 1 1 1 1 1
		1 0 1	X X X 0 0 1 0 0
		1 1 0	X X X 0 0 1 0 0
		1 1 1	X X X 0 0 0 0 0
	0 0 0	0 0 0	X X X
		0 0 1	X X X
0 0 0 0 X 1 1 1	1 1 1	1 0 0	X X X
		1 0 1	X X X
		1 1 0	X X X
		1 1 1	X X X

Character Pattern Example (1)

Cursor Position

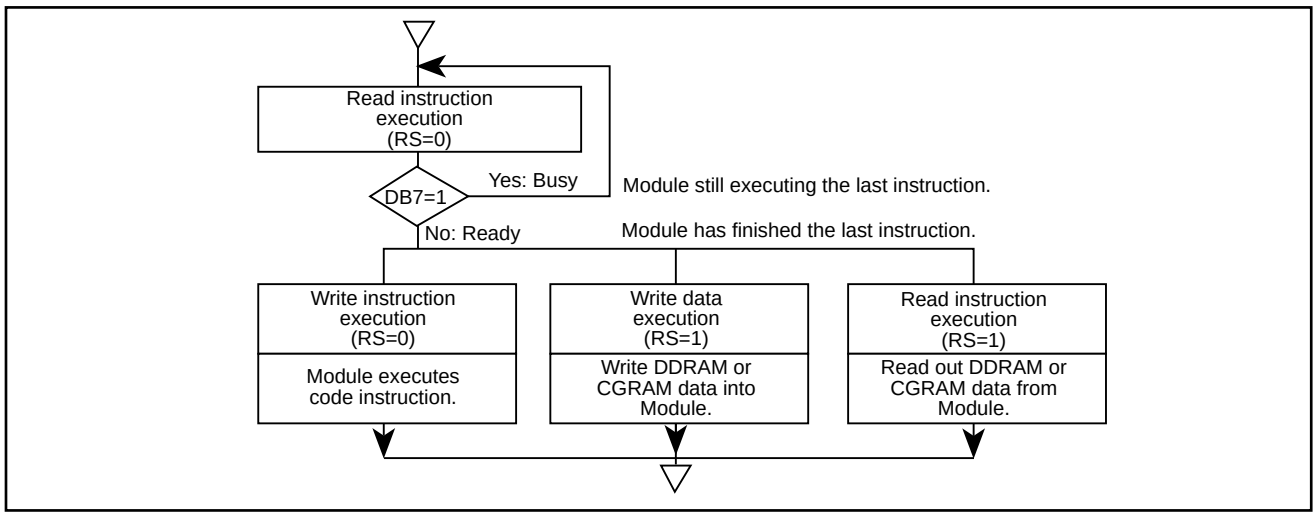
Character Pattern Example (2)

X Don't care

Notes: 1. Character code bits 0~2 correspond to CG RAM address bits 3~5.

2. CG RAM address bits 0~2 define character pattern row address. The 8th row is the cursor position and the display is logically OR ed with the cursor.
3. Character pattern column positions within a row correspond to CG RAM data bits 0~4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5~7 are not used for display, they can be used as general data RAM .
4. CG RAM character patterns are selected when character code bits 4~7 are all '0'. However, since character code bit 3 is a 'don't care' bit, character pattern example 1, for instance, is selected by character code 'Ø0' (hexadecimal) or 'Ø8' (hexadecimal).
5. '1' for CG RAM data corresponds to pixel displayed (ON) and '0' pixel absent (OFF).

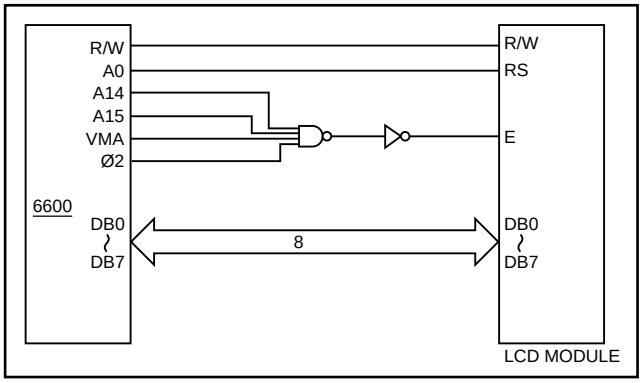
Interfacing with microprocessors



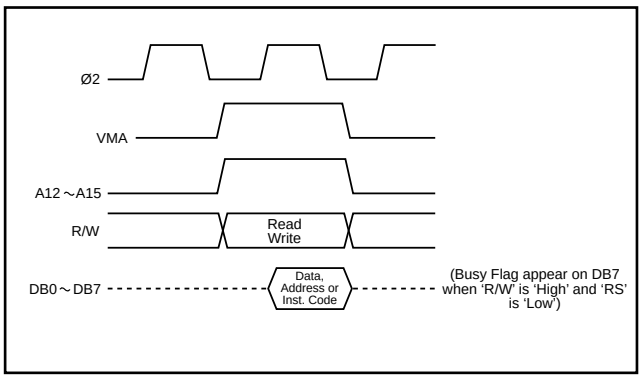
Notes: 1. In this flowchart, Read and Write instructions correspond with external RAM reference instruction or I/O instruction.

2. By providing sufficient instruction execution time, it may be unnecessary to monitor the 'Busy Flag.

Interface with 6800



Timing chart

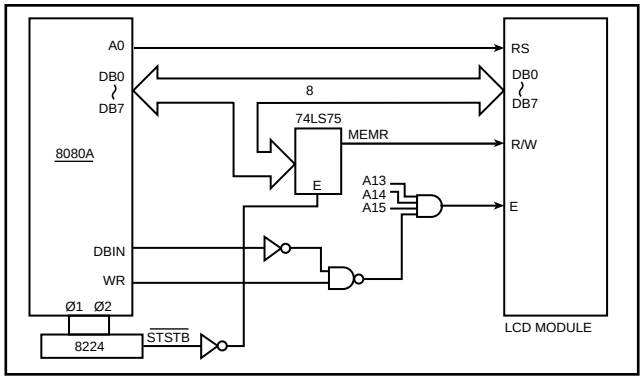


- 6800
- LCD module is treated as an I/O or RAM device
- A_0 is connected to RS and hence its level selects either the instruction register or the data register
- The addresses of the module (as I/O) in the address map of the 6800 are:

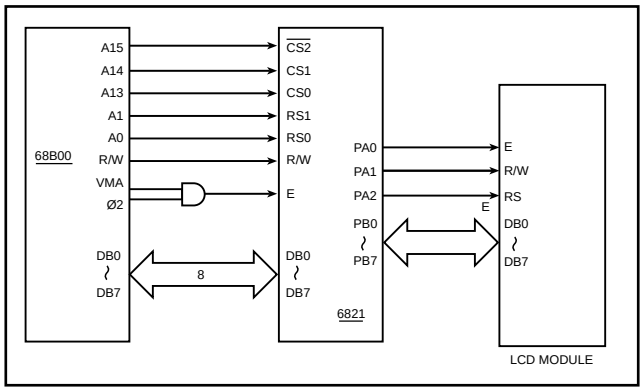
Write function	# 'FXX0' (R/W = 0)
Write CGRAM/DDRAM data	# 'FXX1' (R/W = 0)
Read Busy flag/address	# 'FXX0' (R/W = 1)
Read CGRAM/DDRAM data	# 'FXX1 ' (R/W = 1)

Note: The lead bit 'F' may be 'C', 'D', or 'E', X = Don't care.

Interface with 8080A



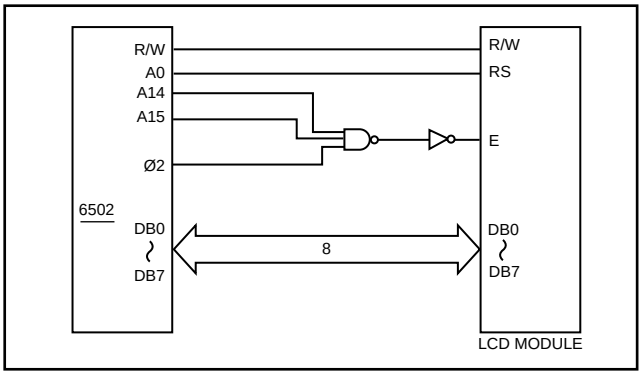
Interface with 68B00



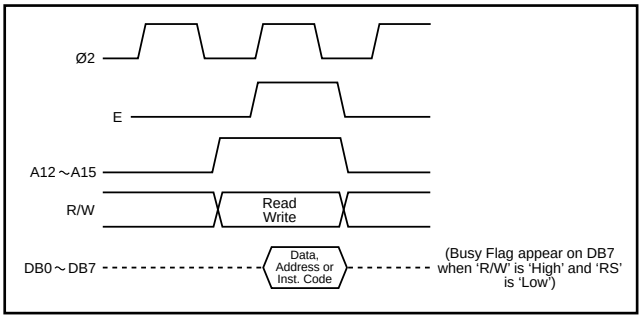
- 68B00

The 68B00 is a high speed version of the 6800. The 02 signal is too narrow to drive the LCD module correctly. A simple interface uses the 6821 PIA between the CPU and module. This, in conjunction with appropriate user provided software, provides an E pulse of adequate width.

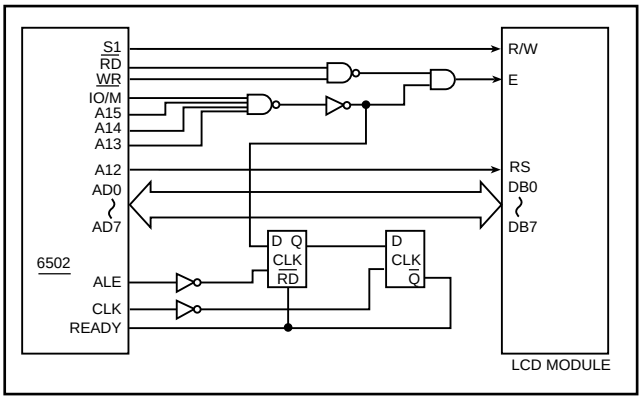
Interface with 6502

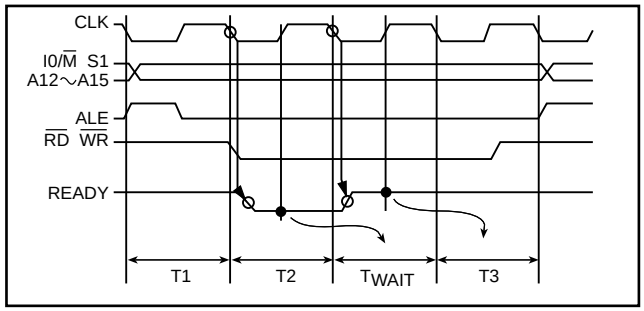


Timing chart



Interface with 8085A





- LCD module is treated as an I/O or RAM device
- The E pulse to the module should be 450nsec min. The RD and WR pulses of the 8085A are specified as 400nsec min and hence need to be lengthened by a slower clock or by the addition of wait states
- The addresses of the module as I/O in the address area of the 8085A are:

Write function	# 'EX' (R/W = 0)
Write CGRAM/DDRAM data	# 'FX' (R/W = 0)
Read busy flag/address	# 'EX' (R/W = 1)
Read CGRAM/DDRAM data	# 'FX ' (R/W = 1)

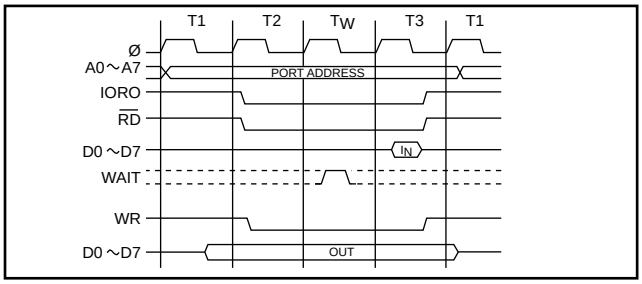
X = Don't care

- 6502
- LCD module is treated as a RAM device
- A_o is connected to RS and hence its level selects either the instruction register or the data register
- The addresses of the module in the address map of the 6502 are:

Write function	# 'FXXØ (R/W = 0)
Write CGRAM/DDRAM data	# 'FXX1' (R/W = 0)
Read busy flag/address	# 'FXXØ (R/W = 1)
Read CGRAM/DDRAM data	# 'FXX1 ' (R/W = 1)

Note: The lead bit 'F' may be 'C', 'D', or 'E'.

Interface with Z-80



- The module is treated as an I/O device

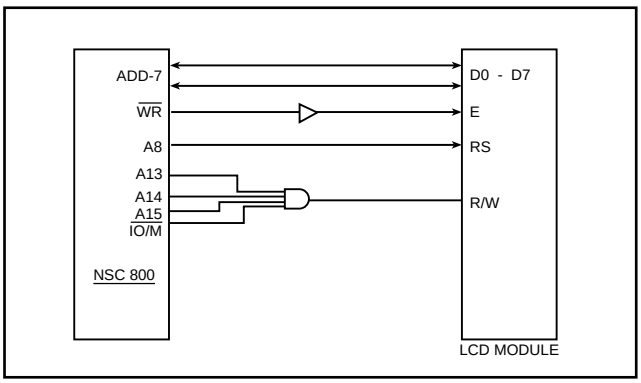
l When accessing I/O, a wait state is inserted automatically by the Z80 and the OR of RD and WR can be at least 450nsec and hence could drive the E input directly. R and C need to be selected to ensure the setup time restriction is met

- If the module is treated as RAM, the user must insert a wait state
- The addresses of the module as I/O device in the address area of the Z-80 are:

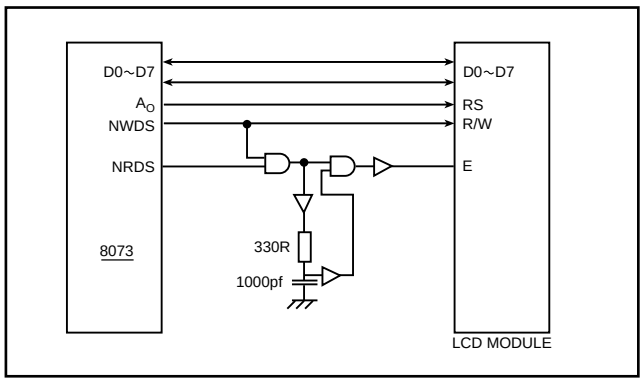
Write function	# 'EX' (R/W = 0)
Write CGRAM/DDRAM data	# 'FX' (R/W = 0)
Read busy flag/address	# 'EX' (R/W = 1)
Read CGRAM/DDRAM data	# 'FX ' (R/W = 1)

X = Don't care

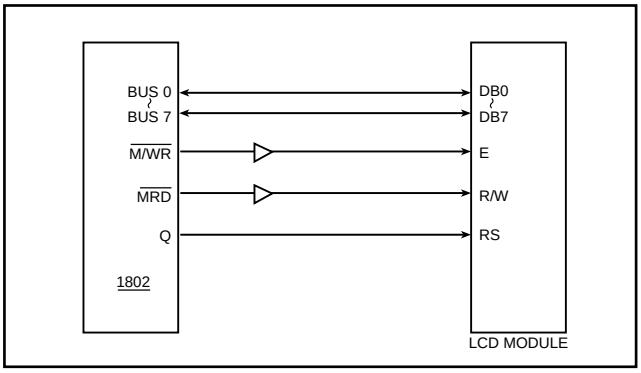
Interface with NSC 800 CMOS micro



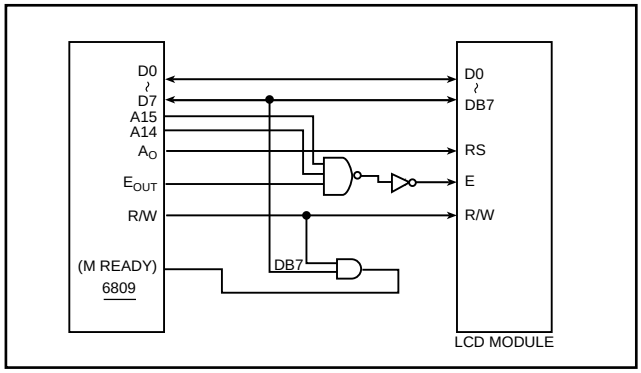
Interface with NSC 8073
Tiny Basic micro-interpreter



Interface with Hughes/RCA 1802 CMOS micro



Interface with Motorola high performance 6809



Handling precautions

1. The polarisers in the panel are easily scratched. Do not touch, press or rub the display panel with hard tools such as tweezers.
2. Do not use organic solvents to clean the display panel as they can cause deterioration of the polarisers.
3. Do not remove the LCD panel from the main unit.
4. Never use or store the LCD module under conditions of abnormally high temperature and humidity.
5. Static electrical charges can damage CMOS/LSI circuitry. Observe normal anti-static handling procedures.

Operation of the **RS** alphanumeric dot matrix modules

Common problems

1. Transmitting too fast to the display:
   a) upon initialisation allow 15ms before sending data,
   b) after transmitting hex 01 or 02 allow 1.6ms,
   c) after all other data allow at least 40µs.
2. Not generating a positive going enable pulse at least 450ns wide.
3. Data, RS and R/W signals are not stable for the minimum set-up and hold times before, and after, the falling edge of the enable pulse (Figures 7 and 8).
4. V_O pin voltage level incorrect – should be 0.7 volt approximately.
5. Display mis-connection: crossed, open or incorrectly terminated cable.
6. LCD input assumed to be configured as an IC.
7. Failure to properly initialise the display.
8. Signal levels too low at the display. Ensure that at least 2.4V (H) is present.
9. Data bus contention. More than one external bus device selected.
10. Not all data bus components have TTL type outputs causing conflict with the on board databus.

Troubleshooting

1. Display appears blank: check +5V and gnd at display: check common problems 4, 5, 6 and 7.
2. Displayed characters enter unreliably or at random: check common problems 1, 3, and 9.
3. Same symptoms as (b) but system has multiple components tied to the data bus: check common problems 8, 9 and 10.

Operational notes

1. Never connect or disconnect the LCD module from the main system whilst power is applied.
2. If the operating temperature falls below the temperature limit, the flashing speed of the display will decrease. If the temperature exceeds the prescribed limit, the display will turn black. Operation returns to normal when the temperature returns to within the normal limits.
3. Adjust V_O for optimum display contrast. (0.2-0.7V.)

Bus connections

The data bus is a 'pseudo' tri-state. There is no means to deselect the display microprocessor. In the absence of an external TTL output device the display will 'pull' the data bus up to +5V. Each bit of the data bus can source up to 0.2mA at a VOH of 2.4V.

The display can be directly connected to a shared data bus if each bus accessing component can legitimately sink 1.5mA with its output low. In this manner the selected device will dominate and the bus operation will be correct. This current sinking specification is standard with TTL-type bus output.

Some all-CMOS systems may not have an adequate 'pull-down' capability. In this instance a tri-state buffer should be used between the system data bus and the display. This buffer would then be selected to access the display.

A similar, PMOS type source is used on the E, RS and R/W lines but as these signals are not generally 'bussed', the effect should not cause any difficulty.

Display operation

The display area is a 16 or 40 character width 'window' on a continuous 80 character RAM. The window displays the first 16 or 40 characters of the RAM depending on the module type. The shift instruction permits the display window to move across the RAM. At 1 to 3Hz, shifts cause the display to scroll and higher speeds give the appearance of the message to be overwritten. During a shift, only the window position alters, not the display memory. The RAM addresses range from 80 to CF (hexadecimal) with 80 being the origin (home).

External electronics communicate with the display using the data bus and only 3 control lines, RS, R/W and E. A data transfer is only required when the external CPU needs to update or read the display and hence only minimal demands are placed on the external system.

RAM and ROM integration

Most applications will employ ROM and RAM in combination. The ROM will usually contain the display initialising codes, fixed format messages, and addressing instructions. The RAM will contain 'live' data which may change. In a CPU system memory devices will normally be 'selected' to access the data bus. Alternatively, dedicated, hardware only, designs can employ counters which 'steer' the bus control between ROM and RAM. Data selectors may also be employed between memory data lines and the display. In either case bus contention must be avoided. Set-up and hold times must be maintained by all components which may eventually 'talk' to the LCD display.

Reading the display

Reading the display consists of monitoring the 'busy flag' and examining the contents of any location within the display data RAM. The busy flag is first read to determine the earliest time that the display module can accept new instructions. The data bus is then read to recover the required information, verify its correctness, or determine any need for a display update. This feature may eliminate the need for external RAM, as single line displays have 40 to 64 locations not displayed which can be used as general purpose RAM.

The busy flag is read by setting RS = R/W = 1 and pulling the enable line high. The flag appears on D7 and is active high. Any write attempted to the module before the busy flag has been cleared to a Low state may be ignored or corrupted with the possibility of error.

The display data is read by first executing a display data address set instruction (RS = R/W = 0), and then by setting RS = R/W = 1. The data bus will contain the valid data on the trailing edge of the enable pulse. The display data address is automatically incremented to allow consecutive 'reads' to read a data block easily.

Sending character strings

Messages may be shown in several ways. Most applications will require a new message to replace an existing one.

Each message to be displayed should be preceded with a 'Clear Display' instruction (Δ1 hexadecimal). Following the 1.6ms set up delay, the message can be input. After the last character has been entered, the display is then 'idled' by either preventing further enable pulses, setting RS = 1 or by sending a code which has no effect, ΔE (hexadecimal) for instance.

Alternatively, multiple messages may be stored in the Display RAM in one data transfer. Rapid shift codes can be used to rotate each new message into the window. To ensure that extraneous characters do not appear in the window when this mode is used, surround each message with an appropriate number of blanks.

Viewing angle control

RS LCD modules are best viewed from slightly below the 'Head-on' viewing angle and hence are ideally suited to keyboard/display units where an angled display enclosure is inconvenient. Single line displays have an optimum contrast ratio about 20 degrees off the perpendicular. Two line versions shift the visual cone about 15 degrees further.

VO of the module allows individual viewers to optimise the display contrast to their particular taste and position and it should be connected to a variable voltage of 0.2 to 0.7V.

Levels higher than these shift the viewing angle so far that the display may be unreadable. There is no benefit in returning the voltage control to a negative potential.

The best technique in maximising contrast is to adjust the contrast control with some characters on display. Turn the control just to the point where undesired dots (those not part of a display character) become invisible.

Note: This does not produce the darkest dot. Adjusting for darkest dots overemphasises the undesired dots resulting in loss of contrast ratio.

Display initialisation

It is always recommended to follow an initialisation routine before using the display to ensure that the display processor has correctly formatted the display window and that it can correctly interpret further instructions.

A suggested sequence to set up an automatically incremented display with steady line cursor follows:

RS = R/W = 0.

8 bit, 1 line, 5×7

3Ø, 3Ø, 3Ø, Ø6, ØE, Ø1

8 bit, 2 lines: 5×7 only

38, 38, 38, Ø6, ØE, Ø1

It is possible to write to just one line of a two line display. Using the '3Δ' instruction will improve the contrast by eliminating line 2.

Four bit machines may also incorporate the display module. Initialisation is critical and this format should be closely followed. As 4 bit operation requires that data be sent twice over the D4-D7 bus, memory requirements are doubled. An advantage is the ability to store all 4 data bits, RS, and R/W in a standard 8 bit wide memory. The 8 bit data bus mode will require at least 9 bits of memory. (Assuming R/W is held low.)

4 bit, 1 line, 5×7

3, 3, 3, 2, 2, Ø, Ø, 6, Ø, E, Ø, 1

* (The single terminating 1 is crucial).

For 2 lines change the repeated 20 code to repeated 24 or 28. i.e. 3, 3, 3, 2, 2, 8, Ø, 6, Ø, E, Ø, 1 etc.

Key operational codes

These are key operational codes which are decoded by the Instruction Register. As these codes are commands they are sent with RS = R/W = 0.

Description	Code
Clear display	Ø1
Home display	Ø2
Direction of next character entry:	
Left	Ø4
Right	Ø6
Display shift with data entry:	
Left	Ø7
Right	Ø5
Cursor:	
On	ØE
Off	ØC
Flash	ØD
Shift left	1Ø
Shift right	14
Display control:	
On	ØE
Off	ØA
Display shift, no data entry:	
Left	18
Right	1C
Display data addresses:	
Home position	8Ø
Rightmost, top	8F(16), A7 (40 char. display)
Linefeed and C.R. To 2nd line	CØ
Rightmost, bottom	CF(16), E7(40)

Programming CG RAM

The character generator (CG) RAM allows 8 custom 5 ¥ 8 characters. Once programmed, the newly created symbols are accessed exactly as if they were in ROM. As the RAM is a volatile memory power must be maintained. The programming format may be programmed into external ROM and sent following display initialisation. All dots of the character matrix may be programmed, including the cursor position, if desired.

The module's RAM is divided into 2 parts: display data and custom graphics. The CG portion of RAM is located between hex 40 and 7F, and is continuous. Locations 40-47 hold the 1st CG character, 48-4F the 2nd, 50-57 the 3rd, and 78-7F the 8th. If, during initialisation, the display was set to automatically increment, then only the single address, 40 need be sent. Adjacent row data will automatically appear at 41, 42 etc. All 8 CG characters may therefore be programmed with the single initial address entry 40 and 64 data writes.

CG RAM is 8 bits wide although 5 bits fill a CG row. The leftmost dot of the CG row corresponds to D4, in the most significant nibble, with the other 4 dots in the least significant nibble (D3-D0). D0 corresponds the rightmost dot. Thus 1F = all dots on. ΔΔ = all dots off, 15 (HLHLH) = 3 dots on, ΔA (LHLHL) = 2 dots on. In each case, 5 bits of the 8 bit code program one row of a CG character. When all 8 rows are programmed, the CG character definition is complete. For example:

RS	R/W	Data	Display	Description
Ø	Ø	4Ø		addresses 1st row, 1st CG character
1	Ø	11	* *	result of 11, 1st row
1	Ø	ØA	* *	result of ØA, 2nd row
1	Ø	1F	*****	result of 1F, 3rd row
1	Ø	Ø4	*	result of Ø4, 4th row
1	Ø	1F	*****	result of 1F, 5th row
1	Ø	Ø4	*	result of Ø4, 6th row
1	Ø	Ø4	*	result of Ø4, 7th row
1	Ø	ØØ		result of ØØ, 8th row (cursor position)
1	Ø	15	* * *	1st row, 2nd CG character. **Note:** Addressing not now required, hex 48 is next in the sequence.

Additional software control

Additional effects can be created by alternating certain codes, exploiting the CG RAM, or altering the system timing. For example:

Flash the display screen

Send the message to the display and then alternate the codes ΔA and ΔE. The period of ΔA will determine the length of time the display is off. This is an effective warning condition.

Flash a selected display zone

Send the desired message noting the display address of the leading character in the zone. Send the address of the lead character and then hex 2Δ for each remaining flashing position. Wait an appropriate time and then rewrite the flashing data. Repeat. While somewhat tedious, the technique is visually effective. A dedicated subroutine could be used to achieve this function.

Scroll the display

Single op codes shift the display left, right, or together shift, and enter, new data. Codes 18, 1C, Δ7, and Δ5 are used. A single line display has an 8Δ character ram allowing the user to 'fill' the ram and then 'step' the data either left or right. Vertical scrolling, where entire 'chunks' of display screen size data are sequentially viewed, can be achieved with a reasonably simple host MPU subroutine.

Create multi-channel bar graphs

Bar graphs are relatively easy to create. The linear bar graph is an excellent trend indicator and can greatly enhance operator feedback. Up to 3 bar graphs can be simultaneously displayed. The CG RAM is programmed with double dot-thickness rows. Blank rows separate each bar, with dots filling rows 1, 2, 4, 5, 7 and 8 of each CG RAM character. 3 graphs use 7 CG RAM characters. The CG is programmed to contain all 3 bars, 3 combinations of 2 bars, and 3 single bars. The host MPU measures each input channel and outputs the appropriate CG RAM character, one at a time. The consecutive RAM characters create the bar of the graph. Single or dual channel graphs are similarly derived.

4 bit operation

Four bit operation has been discussed under 'Display Initialisation'.

The four bit data bus mode will be particularly suitable if:

1. a 4 bit MPU is in use.
2. Insufficient I/O lines are available to support an 8 bit wide bus.
3. Operation direct from an 8 bit EPROM or RAM is required. (At least 9 bits are needed if an 8 bit bus is employed.)

D7-D4 are used during 4 bit data transfers. D3-DΔ may float. The 8 bit hex code is sent one nibble at a time, with the most significant nibble leading.

The 4 bit data mode is particularly suitable when the module is to be driven directly from an EPROM/counter combination, as RD and R/W can be programmed alongside the data. Care must be taken to ensure that RS is correct during each part of the instruction. An easy way to ensure that RS is correct when programming an 8 bit wide EPROM is to make D4 = RS and use 3Δ-3F (hexadecimal) for character data and 4Δ-4F (hexadecimal) for commands.

Code	Character	Command
Ø	0	@
1	1	A
2	2	B
3	3	C
4	4	D
5	5	E
6	6	F
7	7	G
8	8	H
9	9	I
A	:	J
B	;	K
C	<	L
D	=	M
E	>	N
F	?	O